ABSTRACT

A new Static Random Access Memory (SRAM) cell using Thin Film Transistors (TFT) is disclosed. In a first embodiment, an SRAM cell comprises a strong inverter and a strong access device constructed on a semiconductor substrate layer, and a weak inverter and a weak access device constructed in a semiconductor thin film layer located vertically above the strong devices. The strong devices are used in the data read and write paths, and the weak devices are used for latch feed-back and sector data erase. This first embodiment is used for high density and high speed memory applications. In a second embodiment, an SRAM cell comprises thin film inverters and thin film access devices constructed in a semiconductor thin film layer located substantially above logic transistors. The TFT SRAM cell is buried above the logic gates of an Integrated Circuit to consume no extra Silicon real estate. This second embodiment is used for slow access and Look-Up-Tables type memory applications.